**2016 Rover Battery System**

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**Introduction**

The battery system for the 2016 rover encompasses everything necessary for the battery pack’s operation, which includes the battery management system, the battery charger, and the battery cells themselves.

**Battery Pack**

**Battery Management System**

Lakdjflasdjflaksj

**Requirements**

Asdflkjasldkfj insert info about cell measurements, current measurements, balancing current, state of charge and state of health calculations here

**Monitoring Analog Front-End**

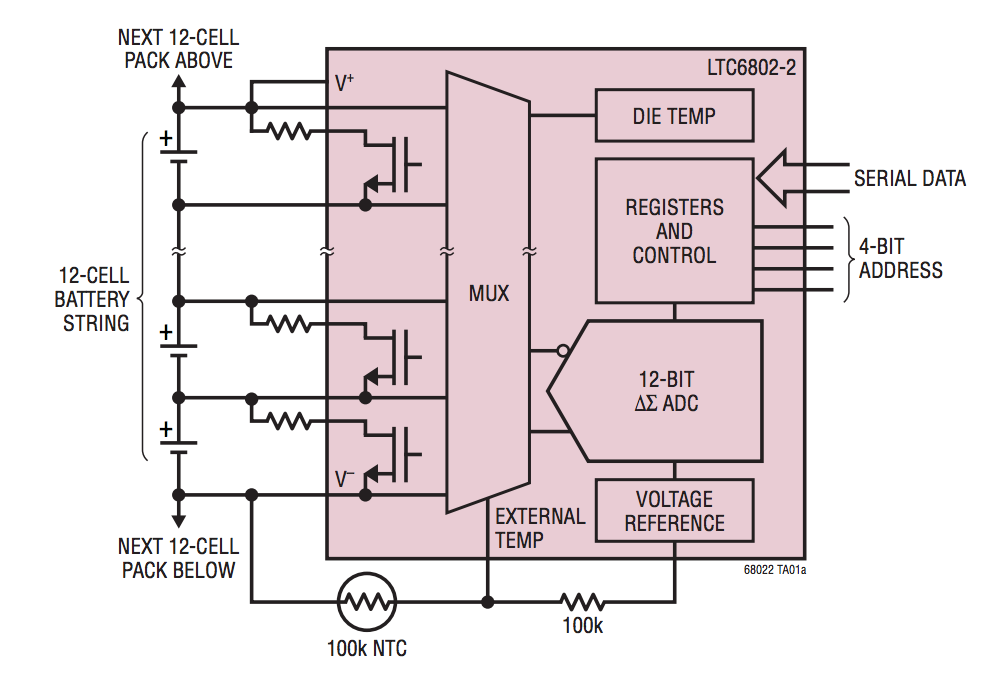
The BMS must make a large number of sensitive analog measurements to function properly, including voltage, current, and temperature measurements. Additionally, in order to perform cell-balancing, the BMS must drive a large number of balancing switches. Due to the sheer number of analog measurements that are necessary, it is impractical to make all of these connections directly to a microcontroller unit’s ADC. The analog data sources proposed for this system are listed in table 1 below.

|  |  |  |
| --- | --- | --- |
| **Data Source** | **Number of Independent Measurements** | **Voltage Measurement Range (V)** |
| Cell Voltage | 8 to 12 (same as number of cells) | 0 to 4.5 (absolute limit)  2.5 to 4.2 (typical) |
| Pack Current | 1 | -5 to 5 (dependent on sensor) |
| Pack Voltage | 1 | 0 to 50 (scaled to 0 to 5 or 0 to 3.3) |
| Charger Output Current | 1 | - 5 to 5 (dependent on sensor) |
| Charger Input Voltage | 1 | 0 to 50 (scaled to 0 to 5 or 0 to 3.3) |
| System Output Voltage | 1 | 0 to 50 (scaled to 0 to 5 or 0 to 3.3) |
| Temperature | 2 | 0 to 3.3 or 0 to 5 |

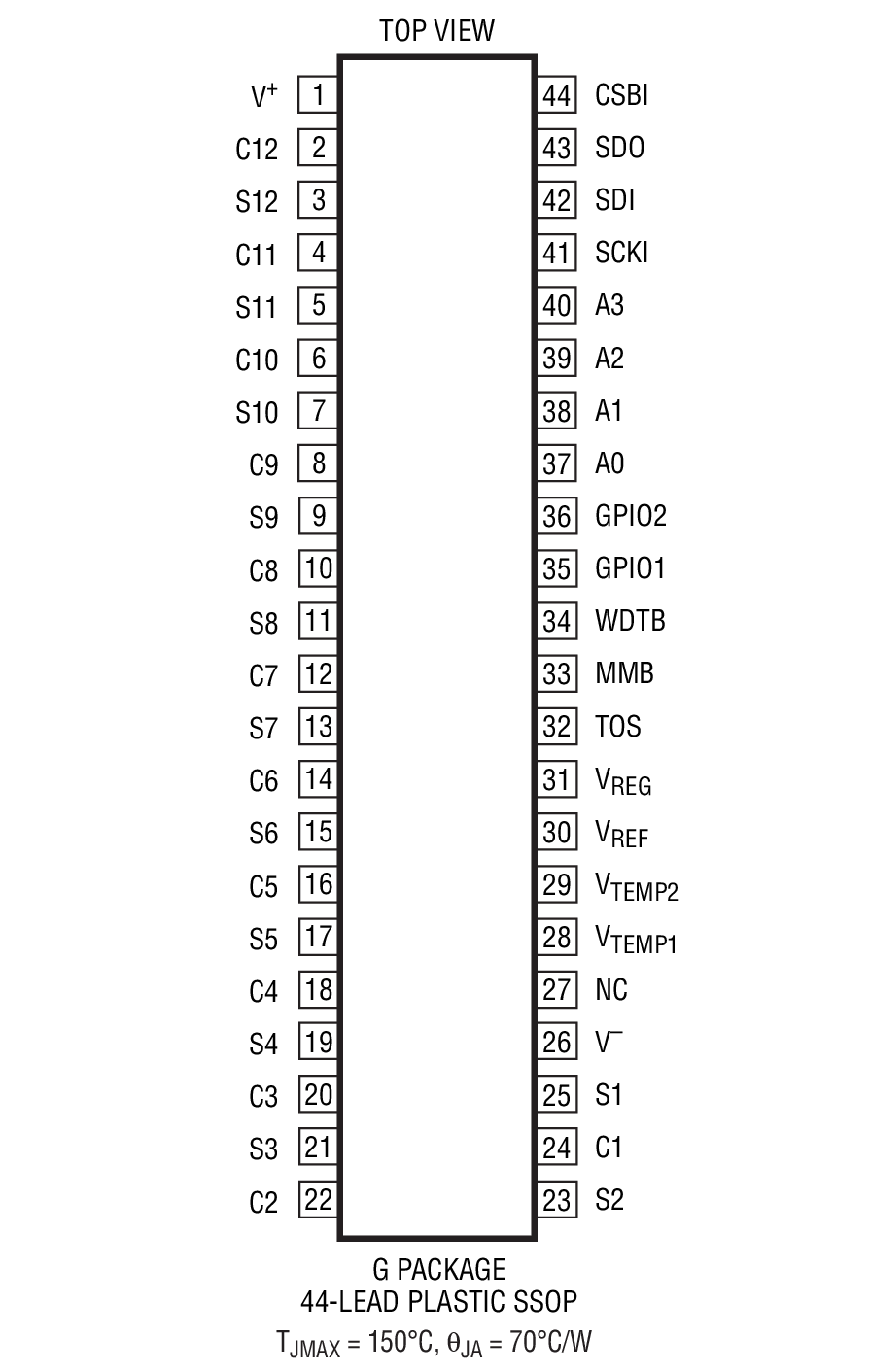
**Table 1 –** Analog Data Sources Measured by the BMS.

Since as many as 19 different analog data sources may be measured by the BMS at any given time, it is necessary to multiplex the channels of the master microcontroller’s ADC. High quality analog multiplexers are often expensive, however, and require this approach requires the microcontroller to dedicate processor cycles to MUXing and analog-to-digital voltage conversion. Additionally, it poses a safety hazard by potentially exposing the low-voltage electronics of the microcontroller to full pack voltage (potentially over 50V). An alternative solution to a multiplexer is the use of a dedicated analog front-end ASIC that would make measurements, perform analog-to-digital conversion, and provide an isolated digital interface to the microcontroller.

Linear Technology’s LTC6802 Battery Stack Monitor IC has been selected for this application [13]. As an analog front-end IC, it can measure 2 to 12 cell voltages, perform passive balancing on 2 to 12 cells, and measure temperature from two external temperature sensors. It is daisy-chainable if additional measurements are necessary and provides a serial data interface to the master microcontroller. Figure 1 shows a high-level overview of the IC’s typical application. Figure 2 shows the IC’s pinout.



**Figure 1 –** Typical Application of the LTC6802-2.

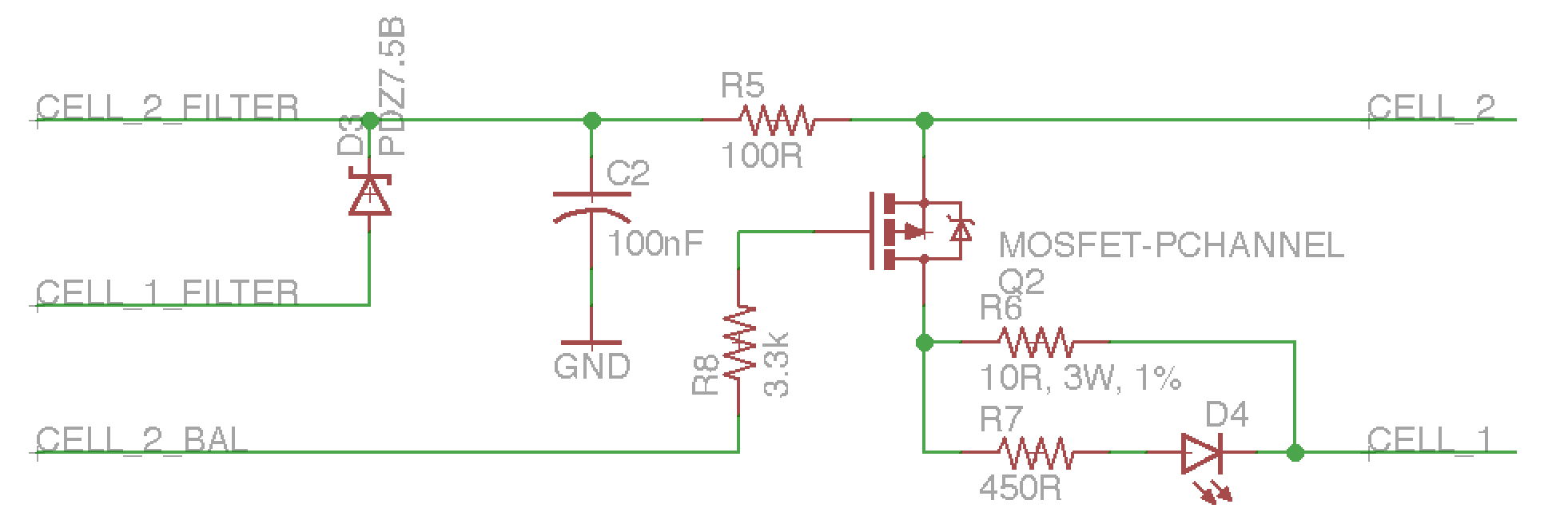


**Figure 2 –** Pinout of the LTC6802-2.

For the purposes of this application each connection between a cell module and the IC consists of a one-pole RC filter, transient voltage suppression circuit, and an off-IC balancing circuit. An example of one such circuit is shown in figure 3 below. This circuit is repeated for each of the eight cell modules in the pack.

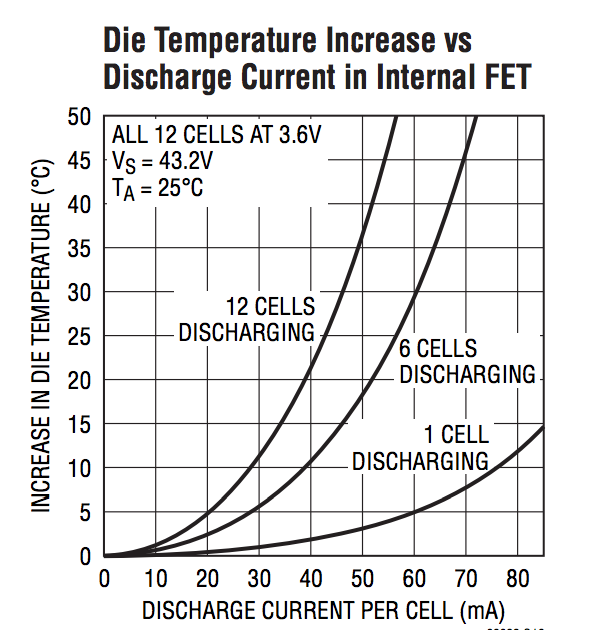
The RC filter is used to suppress noise in the cell voltage measurements that is common when the pack is exposed to load transients. Values of 100 Ohms for the resistor and 100nF for the capacitor were selected to produce a low-pass filter with a cutoff frequency of approximately 16kHz. A large capacitor was not used in order to allow the LTC6802 IC to more easily detect cell measurement line disconnections [13].

A simple zener diode between cell filter nodes serves as transient voltage snubber circuit.

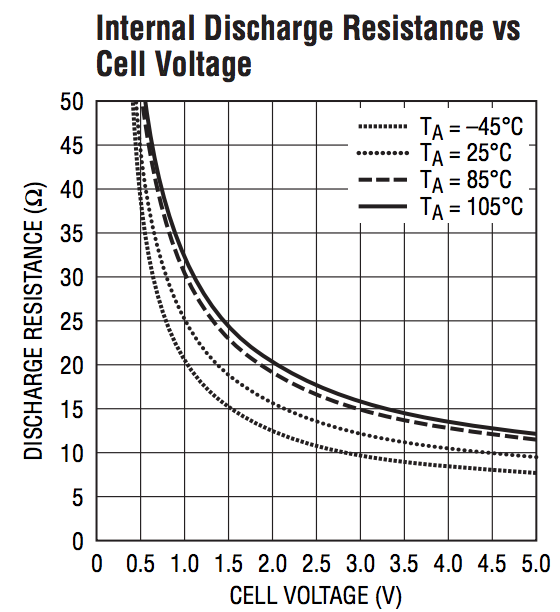


**Figure 3 –** Cell Module Interface Circuit.

Finally an external MOSFET and power resistor were included for passive cell balancing. Although the IC is capable of performing balancing without external hardware, its maximum balancing current is limited to 50 to 100mA (depending on the exact balancing conditions). This is due to the IC’s thermal dissipation characteristics, as shown in figure 4. The IC’s typical internal cell discharge current may be determined from the graph in figure 5.



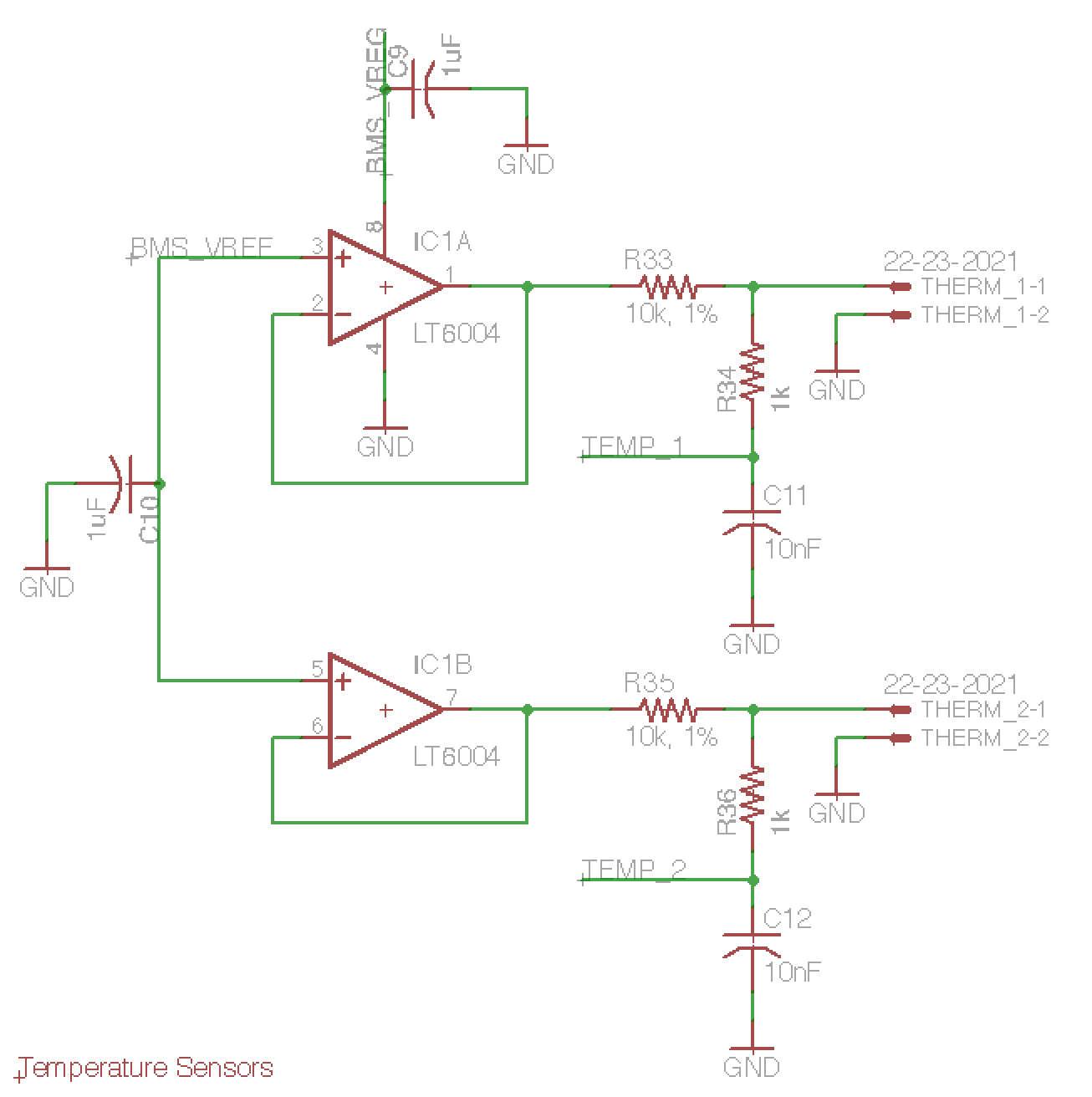
**Figure 4 –** LTC6802 Temperature Characteristics vs. Cell Discharge Current.



**Figure 5 –** The LTC6802’s Internal Discharge Resistance vs. Battery Cell Voltage.

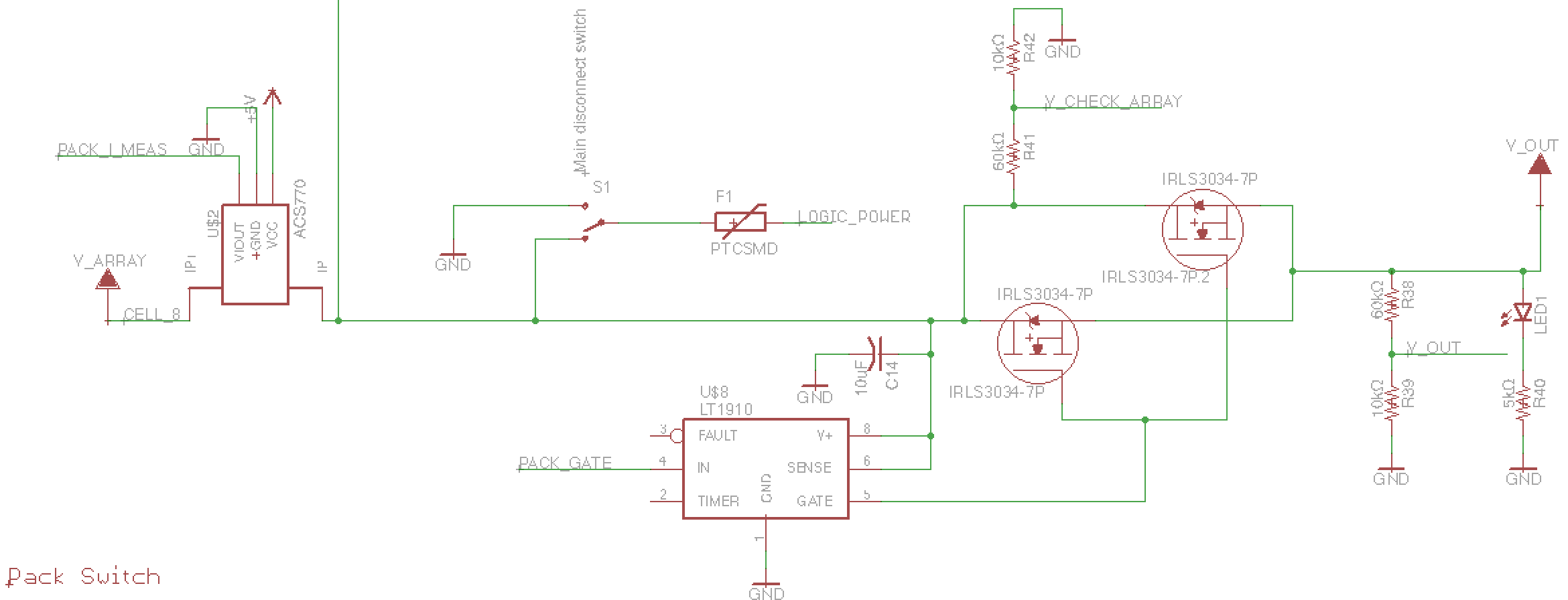
The external balancing circuit consists of a small SOT23 package P-Channel MOSFET driven by the LTC6802 IC and a 10-Ohm, 3W, through-hole power resistor. For a cell voltage of 4V, this allows for a balancing current 400mA without overheating issues. Additionally, a small LED is connected in parallel to the power resistor to provide a visual indication that the balancing circuit is active.

For the purposes of battery pack thermal monitoring (and with cooling fans, management) two external NTC thermsistors may be connected to the LTC6802 IC as shown in figure 6. The NTC is connected in a voltage divider configuration to the IC’s analog voltage reference and measured by its on-board ADC. A voltage buffer circuit is included between the IC’s analog reference and the temperature sensor in order to better support a range of NTC resistor values. The “Temp\_1” and “Temp\_2” nets are connected to the IC’s temperature VTEMP1 and VTEMP2 pins, respectively.



**Figure 6 –** Supporting Circuitry for External NTC Thermsistors.

A;fjladksjf Insert info about pack voltage and current measurements here



**Figure 7 –** Pack Current and Voltage Measurements; Load Switch MOSFET.

Afljasdlfj alsk insert info about LTC interface to microcontroller here.

**Microcontroller**

Although the analog front-end IC is useful for aggregating battery pack data, it cannot make decision about the pack on its on. A microcontroller unit is necessary for monitoring pack operating state, activating balancing circuitry, controlling charging, and connecting and disconnecting the pack from its load. The I/O requirements for the microcontroller are summarized in table 2.

|  |  |  |
| --- | --- | --- |
| **Function** | **Type of I/O Port** | **Quantity of Ports/Pins** |
| Analog Front-End Communication | SPI | 1 |
| Cooling Fan Control | PWM | 4 |
| Cooling Fan Speed Feedback | GPIO | 4 |
| Buzzer Alarms | PWM | 2 |
| LED Gauge | GPIO | 4 |
| Emergency Stop Input | Digital Input – Interrupt | 2 |
| Pack Current Measurement | ADC | 1 |
| Pack Voltage Measurement | ADC | 1 |
| Pack Switch | GPIO | 1 |
| Pack Output Voltage Measurement | ADC | 1 |
| Charger Control | PWM | 1 |
| Charger Current | ADC | 1 |
| Charger Input Voltage Measurement | ADC | 1 |
| Serial Debug Port | USB | 1 |
| External Communication | Ethernet | 1 |
| External Power Supply Communication | GPIO | 2 |
| External LCD Screen | GPIO | 11 |

**Table 2 –** Microcontroller I/O Requirements.

In addition to meeting these I/O requirements, the microcontroller needs to operate at sufficiently high speed to frequently monitor the pack’s state, enable/disable balancing, update the charger power converter control loop, and maintain external communications. A microcontroller with a clock speed of at least 16MHz should be capable of this. Additionally, the microcontroller should be low power and capable of entering a low power sleep mode, as it will always be operating once installed in the pack. For ease of prototyping, it is also ideal if a development board is available for the microcontroller.

The MSP432P401R by Texas Instruments meets these requirements. It is part of TI’s MSP432 family of microcontrollers, a hybrid of the ubiquitous ARM architecture and TI’s low power MSP430 architecture. The microcontroller operates at up to 48MHz, meets the I/O requirements (with the exception of not having an on-board Ethernet PHY module), and consumes 90μA/MHz in low power mode [14]. Texas Instruments also produces a low cost development board targeting the microcontroller. The connections between the microcontroller’s I/O ports and the BMS hardware are described in table 3. Only pins made accessible by the Launchpad development board are listed [15].

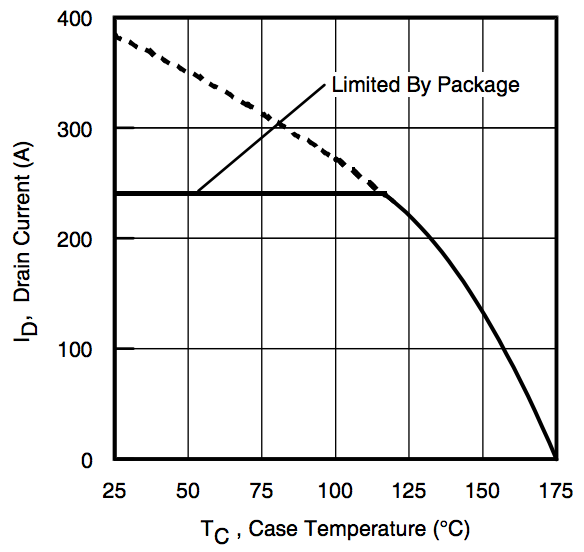
|  |  |  |  |
| --- | --- | --- | --- |
| **Pin** | **Functionality** | **Relevant Hardware Peripherals** | **Connection** |
| 1.5 | Digital Input (Interrupt) |  | E-Stop 1 Input |
| 1.6 | Digital Input (Interrupt) |  | E-Stop 2 Input |
| 1.7 | GPIO |  | External Power Supply Communication |
| 2.3 | GPIO |  | External Power Supply Communication |
| 2.4 | PWM | TA0, CCR1 | Fan 1 Speed Control |
| 2.5 | PWM | TA0, CCR2 | Fan 2 Speed Control |
| 2.6 | PWM | TA0, CCR3 | Fan 3 Speed Control |
| 2.7 | PWM | TA0, CCR4 | Fan 4 Speed Control |
| 3.0 | GPIO |  | Fan 4 Tachometer |
| 3.2 | GPIO |  | Fan 3 Tachometer |
| 3.3 | GPIO |  | Fan 2 Tachometer |
| 3.5 | GPIO |  | LCD Screen RS |
| 3.6 | GPIO |  | LCD Screen R/~W |
| 3.7 | GPIO |  | LCD Screen EN |
| 4.0 | GPIO |  | LCD DB[0] |
| 4.1 | GPIO |  | LCD DB[1] |
| 4.2 | GPIO |  | LCD DB[2] |
| 4.3 | GPIO |  | LCD DB[3] |
| 4.4 | GPIO |  | LCD DB[4] |
| 4.5 | GPIO |  | LCD DB[5] |
| 4.6 | GPIO |  | LCD DB[6] |
| 4.7 | GPIO |  | LCD DB[7] |
| 5.0 | GPIO |  | Fan 1 Tachometer |
| 5.1 | ADC | ADC4 | Charger Voltage |
| 5.2 | ADC | ADC3 | Charger Current |
| 5.3 | ADC | ADC2 | System Output Voltage |
| 5.4 | ADC | ADC1 | Pack Voltage |
| 5.5 | ADC | ADC0 | Pack Current |
| 5.6 | PWM | TA2, CCR1 | Buzzer 1 |
| 5.7 | PWM | TA2, CCR2 | Buzzer 2 |
| 6.0 | GPIO |  | Pack Load Switch |
| 6.1 | Digital Input (Interrupt) |  | Wiznet Data Available Interrupt |
| 6.2 | SPI SS | eUSCI\_B1 | LTC6802 CSBI |
| 6.3 | SPI SCLK | eUSCI\_B1 | LTC6802 SCKI |
| 6.4 | SPI MOSI | eUSCI\_B1 | LTC6802 SDI |
| 6.5 | SPI MISO | eUSCI\_B1 | LTC6802 SDO |
| 6.6 | Digital Input (Interrupt) |  | LCD/LED Indicator On/Off Button |
| 6.7 |  |  |  |
| 7.0 |  |  |  |
| 7.1 |  |  |  |
| 7.2 |  |  |  |
| 7.3 |  |  |  |
| 7.4 |  |  |  |
| 7.5 |  |  |  |
| 7.6 |  |  |  |
| 7.7 |  |  |  |
| 8.0 | PWM | TA1, CCR0 | Charger Power Converter Control |
| 8.2 |  |  |  |
| 8.3 |  |  |  |
| 8.4 |  |  |  |
| 8.5 |  |  |  |
| 8.6 |  |  |  |
| 8.7 |  |  |  |
| 9.0 | GPIO |  | Wiznet Reset |
| 9.1 |  |  |  |
| 9.2 |  |  |  |
| 9.3 |  |  |  |
| 9.4 | SPI SS | eUSCI\_A3 | Wiznet SS |
| 9.5 | SPI SCLK | eUSCI\_A3 | Wiznet SCLK |
| 9.6 | SPI MISO | eUSCI\_A3 | Wiznet MISO |
| 9.7 | SPI MOSI | eUSCI\_A3 | Wiznet MOSI |
| 10.0 | GPIO |  | LED Shift Register CLR |
| 10.1 | GPIO |  | LED Shift Register RCK |
| 10.2 | GPIO |  | LED Shift Register SER\_IN |
| 10.3 | GPIO |  | LED Shift Register SRCK |
| 10.4 |  |  |  |
| 10.5 |  |  |  |

**Table 3 –** Microcontroller I/O Connections. Unused Pins are Shaded.

**Pack Load Switch**

The master microcontroller is responsible for connecting/disconnecting the battery pack from its load by commanding the output of a MOSFET driver IC. The microcontroller will switch the pack off when the battery pack is operating outside of its safe operating area or if the emergency stop button is activated. The hardware responsible for this functionality is shown in figure 7.

In order to handle the 200A continuous discharge the pack is capable of sustaining, as well as larger transient load currents, the load switch consists of two International Rectifier IRLS3034 Power MOSFETs connected with drain and source junctions in parallel [16]. The MOSFETs case temperature characteristics versus drain current are shown in figure 8. Each MOSFET should be capable of handling 200A independently, thus together they should be able to sustain load transients on the order of 400A without significant overheating issues. The MOSFETs are connected in parallel without load balancing resistors because in general they will be operated in the saturation region with low Rdss(on), and thus their negative temperature coefficient properties should ensure proper load current balancing between the two devices [17].

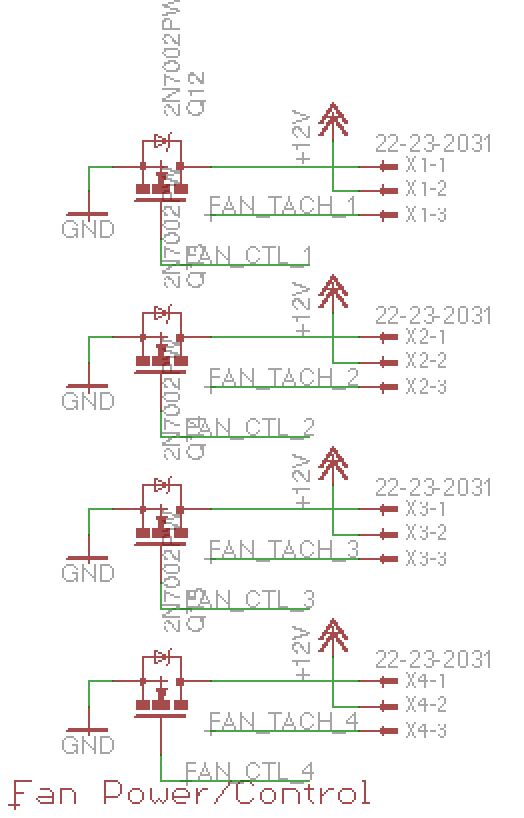


**Figure 8 –** IRLS3034 Case Temperature vs. Drain Current.

The two MOSFETs will be driven by a single LT1910 high side MOSFET driver IC [18]. As the FETs will generally operate in the saturation for long periods of time, turn-on time, and therefore gate driver current and gate charge are not serious design concerns. The ability of this MOSFET and driver configuration to sustain 200A of load current continuously has been empirically verified by the team in past years.

**Cooling Fans**

In order to ensure the battery pack is properly cooled when under heavy load conditions, connections for four external cooling fans have been made available. The four fans can have their speed individual controlled by driving an onboard MOSFET with PWM. Additionally, the master microcontroller can measure tachometer feedback from each fan. The fans are connected to the board via a standard 0.1” pitch three-pin connector. Support hardware for this configuration is shown in figure 9.



**Figure**

**Battery Charger**

An integrated charger for the battery pack is desired in order to charge the batteries at their rated-charging speed and to simplify the charging process for the end-user. The preliminary charger will accept a DC-input greater than pack voltage for a buck-converter based charger. A future revision of the charger could be a buck-boost converter that would also accept charging voltages below pack voltage.

**Charging Requirements**

The selected cells are rated for two charging algorithms: a standard charge and a fast charge. As their names indicate, the standard charging algorithm is slower, but results in increased cell lifetime; while the fast charge is significantly faster but will reduce cell lifetime.

The standard charging algorithm consists of two phases: the constant current (CC) phase and the constant voltage phase (CV). For a standard charge, CC charging first takes place at 1250mA (per parallel cell), then CV charging takes at 4.2V (per series cell) until charging current tapers to 50mA per cell. For a fast charge, CC charging first takes place at 4000mA (per parallel cell), then CV charging takes at 4.2V (per series cell) until charging current tapers to 100mA per cell. After fast charging the batteries must rest for 10 minutes.

Since the fast charging algorithm places the greatest demand on the battery charger, it will be used for determining battery charger requirements. For the proposed 10 parallel/8 series (10p8s) battery pack, the minimum pack voltage will be 20V and the maximum pack voltage will be 33.6V. Thus the charger must be capable of constant voltage charging at 33.6V. Since there are ten cells in parallel, the charger must be capable of sourcing 40A during CC charging. The worst-case power draw on the charger occurs during a 33.6V, 40A charging period (an unlikely load point for the battery pack), which is equal to 1344W. Design goals for the charger are summarized in table 1 below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **Minimum** | **Nominal** | **Maximum** | **Units** |
| Output Voltage | 20.0 |  | 33.6 | V |
| Output Current | 12.5 |  | 40.0 | A |
| Input Voltage | 35 |  | 50 | V |
| Rated Power |  | 1350 |  | W |
| Efficiency | 85 | 95 |  | % |
| Weight |  | 200 | 1000 | g |
| Board Area |  |  | 24 | Sq. in. |

**Table 1 –** Charger Design Parameters

**Buck-Converter Design**

>Include a switching frequency vs. required inductance graph

**Inductor Selection**

The selected inductor is largely dependent on the selected switching frequency for the converter. Higher switching frequencies lead to higher switching losses and create more stringent requirements for the converter’s MOSFET switches and MOSFET drivers, however allow for the use of smaller magnetics. Lower switching frequencies require an inductor of higher rated inductance and thus a larger, heavier inductor. Inductors for various switching frequencies are presented in this section.

Based on the analysis in the previous section, a switching frequency of in the range of 50kHz to 500kHz is likely. The requirements for inductors for frequencies in this range are presented in table 2 below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **50kHz Inductor** | **125kHz Inductor** | **250kHz Inductor** | **500kHz Inductor** |
| Inductance (μH) | 132 | 88 | 44 | 22 |
| RMS Current (A) | 40 | 40 | 40 | 40 |
| Saturation Current (A) | 40 | 40 | 40 | 40 |
| Ripple Current (A) |  |  |  |  |

**Table 2 –** Inductor Requirements for Various Switching Frequencies.

Various suppliers were searched for inductors that meet the above requirements. The selected inductor for each switching frequencies was selected by best meeting the required electrical characteristics while minimizing cost, weight, and size. Possible inductors are presented in table 3 below. Values for the table were derived from the manufacturer datasheet tables and the curves shown in figures 1, 2, and 3.

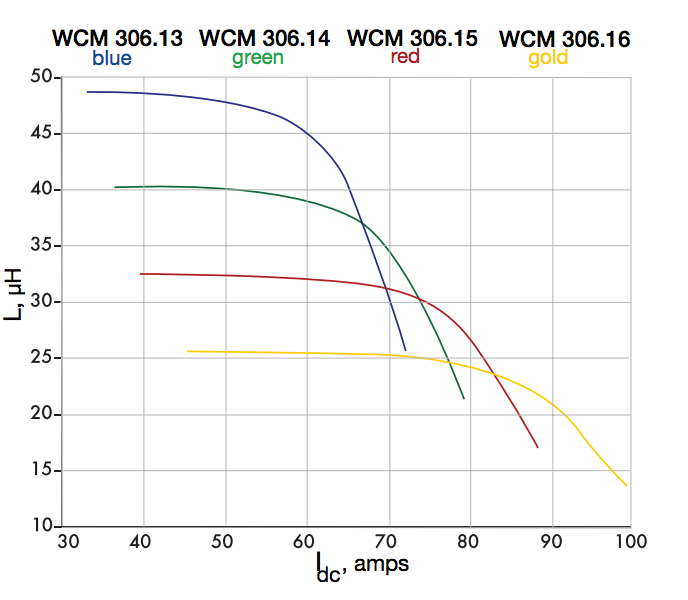
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **50kHz Inductor** | **125kHz Inductor** | **250kHz Inductor** | **500kHz Inductor** |
| **Part Number** | WCM 306-8 | WCM 306-10 | WCM 306-13 | AGP4233-223ME |
| **Supplier** | West Coast Magnetics | West Coast Magnetics | West Coast Magnetics | Coilcraft |
| **Price ($)** |  |  |  |  |
| **Inductance (μH)** | 131 | 91 | 49 | 22 |
| **Inductance Tolerance** |  |  |  | +/- 10% |
| **Weight (g)** | 1000 | 1000 | 1000 | 135 |
| **DCR (mOhms)** | 2.80 | 1.89 | 1.03 | 2.95 |
| **Size - Length, Width, Height (cm)** | 7.75 x 7.24 x 7.62 | 7.75 x 7.24 x 7.62 | 7.75 x 7.24 x 7.62 | 4.22 x 3.58 x 2.80 |
| **RMS Current (A)** | 33.0 | 39.0 | 55.0 | 34.0 |
| **Saturation Current, 10% (A)** | 37 | 45 | 60 | 32.8 |
| **Saturation Current, 20% (A)** | 39 | 47 | 65 | 35.4 |
| **Saturation Current, 30% (A)** | 42 | 50 | 67 | 36.6 |
| **Ripple Current (A)** |  |  |  |  |
| **Temperature (C)** |  |  |  | 125 |

**Table 3 –** Selected Inductor Characteristics for Various Switching Frequencies[1][2].

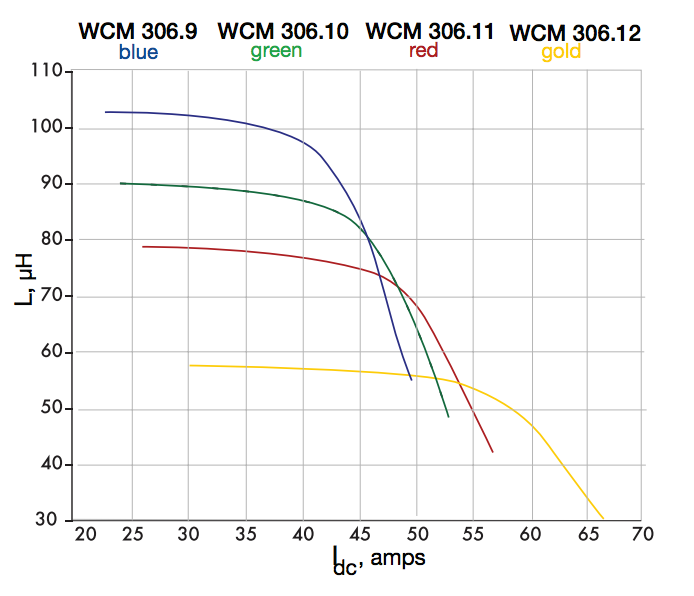
The two best inductors for this application are the WCM-306-10 (a 91uH inductor produced by West Coast Magnetics) and the AGP4233-233ME (a 22 uH inductor produced by Coilcraft).

The WC Magnetics inductor is well suited for this application because it allows for a reasonable switching frequency (125kHz) while still meeting the current requirements of the converter (the 39.0Arms is the limiting current rating; the core will not saturate within the converter’s operating limits). Unfortunately this inductor is quite large, weighing 1kg and having a board surface area of 56.11cm2 (8.70in2). This makes the inductor ideal for an off-rover charger; however, it may prove to be too large for an integrated charger.

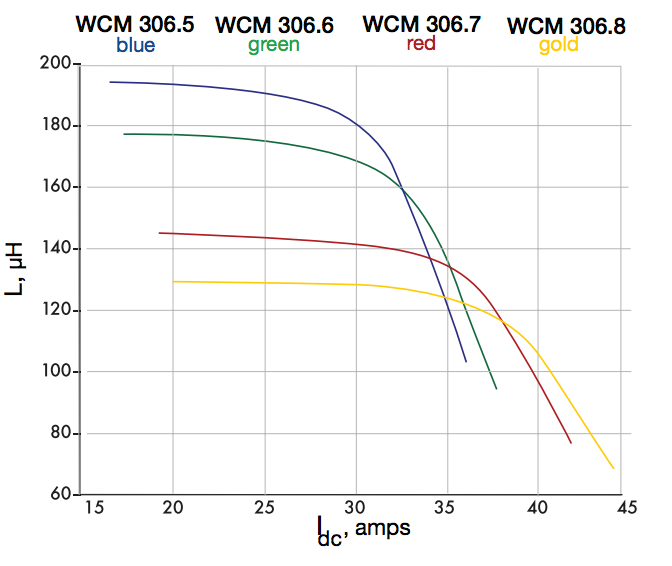
The Coilcraft inductor is also well-suited for this application largely due to small-size. It weighs only 135 grams and uses only 15.10cm2 (2.34 in2) of board space. This is 86% savings in weight and 73% savings in volume compared to the WC Magnetics inductor. Unfortunately this inductor is not capable of supporting the full rated current of the charger, limited by a 34.0Arms current and a 32.8A saturation current for a 10% loss of inductance. (More detailed analysis is required to demonstrate this inductors performance over various charger operating points due to the lower saturation current.)



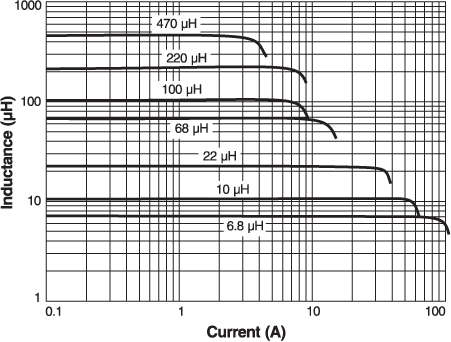
**Figure 1 –** Saturation Current for Inductor WCM 306.13.



**Figure 2 –** Saturation Current for Inductor WCM 306.10.



**Figure 3 –** Saturation Current for Inductor WCM 306.8.



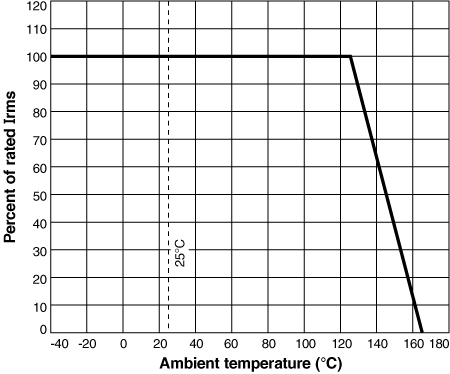
**Figure 4 –** Saturation Current for the Coilcraft Inductors.

There are two major sources of inductor losses: AC-current induced core losses and DC equivalent-resistance heat losses. For each of the selected inductors the core losses are negligible compared to the resistive heating loses, so they are ignored here. The resistive losses may be calculated for both inductors using the maximum RMS current of the charger and the equivalent DC resistance of the inductor:

For the Coilcraft inductor:

For the selected WC Magnetics inductor:

For the Coilcraft inductor, the manufacturer’s website indicates this would lead to approximately a 45°C increase in inductor temperature. Furthermore, the temperature derating curve (*see figure 4*) indicates that this temperature rise would not be an issue for a wide range of ambient temperatures. WC Magnetics does not publish data on their inductors’ thermal resistance, so there is not a direct method to calculate this part’s temperature rise above ambient; however, it is possible to assume it would remain within normal operating conditions as 40A is far below the part’s rated RMS current.



**Figure 4 –** RMS Current Temperature Derating Curve for AGP4233-223ME [3].

**MOSFET Switch Selection**

As discussed in the section on inductor selection, there is a trade-off between switching frequency, inductor requirements, and MOSFET requirements.

For this type of switching converter, the MOSFET is a large source of losses. Losses occur largely in two regions of the switch’s operation: the linear region when the switch is between its “on” and “off” states, and in the saturation region when the switch is “fully on.” Losses in saturation mode are most easily modeled by an equivalent on-state resistance known as the “rds(on).” Losses in the linear mode are more complex to model and much greater than those when the MOSFET is in the saturation region. Therefore it is important to minimize the time that the MOSFET operates in the linear region. This time is dictated by a variety of factors, including gate capacitance, body diode capacitance, and ajlkdfjakd [4]. Additionally the functionality of the MOSFET will depend on its thermal characteristics. Potential MOSFETs for this application are presented in table 4 below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Part Number** | **CSD18532KCS** | **IRFH7191** | **IRFH7188** | **IRFH7185** |
| **Manufacturer** | Texas Instruments | International Rectifier | International Rectifier | International Rectifier |
| **Package** | TO-220 | PQFN 5x6 B/E | PQFN 5x6 B/E | PQFN 5x6 B/E |
| **Price ($/1 unit)** | $2.79 | $2.87 | $2.43 | $3.64 |
| **VBRDSS (V)** | 60 | 100 | 100 | 100 |
| **VGS,Max (V)** | 20 | 20 | 20 | 20 |
| **RDS(on) (mOhms)** | **4.2** | **8** | **6** | **5.2** |
| **Qg (nC)** | **44** | **26** | **33** | **36** |
| **Qgd (nC)** | 6.9 | 8.3 | 11 | 11 |
| **Id @ T=25C (A)** | 100 | 80 | 105 | 123 |
| **Ciss (pF)** | 3900 | 1685 |  |  |
| **Coss (pF)** | 470 | 836 |  |  |
| **Qrr - Diode (nC)** | 127 | 126 |  |  |
| **RΘJC (°C/W)** | 0.6 | 1.2 |  |  |
| **RΘJA (°C/W)** | 62 | 35 |  |  |
| **Q\*R** | 185 | 208 | 198 | 187 |

**Table 4 –** Comparison of potential switching MOSFETS with a Q\*R figure of merit; unit price collected from Digikey [5][6][7][8].

With modern FET technology, the selection of a MOSFET capable of sustaining 40A continuous in the on-state is trivial. A buck-converter by nature, however, will rarely operate with the switching FET continuously in the on-state. During transitions between the on- and off-states the FET will operate in a linear/triode region in which significantly greater switching losses will occur. Therefore, in order to minimize the total switching losses, it is essential that the MOSFET remain in the linear region of operation for the shortest period of time possible. This transition time is dictated by how quickly the gate-to-source voltage can be transitioned by the driver circuit. In ideal conditions, this is nearly instantaneous. A real-world trade off in the construction of high-current FETs, however, is the presence of a significant capacitance at the gate of the MOSFET, which contains a large charge that must be transferred by the driver circuit. For MOSFETs with a large gate charge this can require pulses of many amperes to switch the MOSFET quickly. If this switching transition is not sufficiently minimized, the converter will incur significant switching losses and the MOSFET will overheat. Typically, there is a tradeoff between minimizing the Rds,ON and the gate charge of a MOSFET. Additionally, some manufacturers produce MOSFETs with low gate charges specifically for high-speed switching applications.

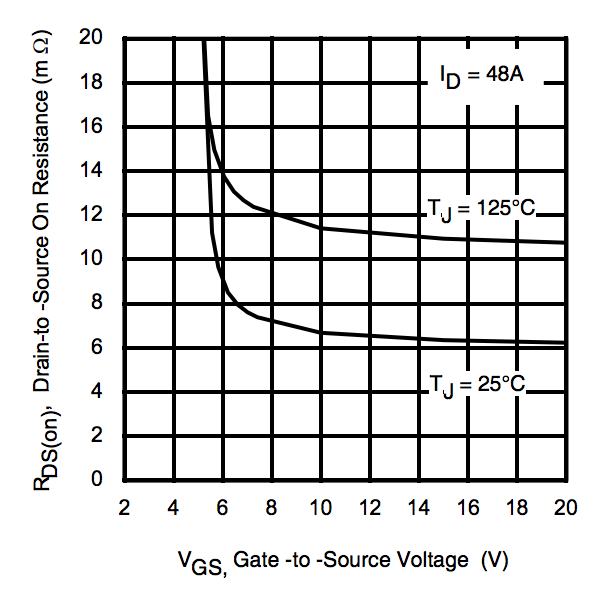
Of the MOSFETs listed in table 4, the IRFH7191 is best suited for this application. All of the MOSFETs have a similar Q\*R figure of merit, which indicates the switches performance for both minimizing loss during operation in the saturation region and it ability to be switched between the on and off states quickly so as to minimize time in the linear region of operation [12]. As the RDS(on) values of all the MOSFETs were appropriate for this application, the 7191 was selected for its especially low gate charge and input capacitance; allowing it to perform well during high speed switching.

Power losses in this switch may be estimated by analyzing its performance independently in two operating regions: the linear/triode region during switching; and the saturation region during its on-state [4]. In the on-state the MOSFETs losses may simply be modeled as a series resistance, equal to the value of RDS(on) provided in the datasheet. It is important to note that the value of RDS(on) also varies over temperature, so it is important to account for this in analysis. This characteristic is shown in figure 5 below.

Assuming that the driver circuit ensures MOSFET operation in full saturation (by ensuring VGS is greater than approximately 8V), then at 25°C it is reasonable to assume an RDS(on) of approximately 6.5mΩ, and at 125°C it is reasonable to assume an RDS(on) of 11mΩ. Note that there is a significant increase in switching losses as the FET’s temperature increases. Standard full-load conditions for this charger are specified to be 40A (although lower limits may exist for some inductors due to core saturation). Using these values, the power loss in the FET may be calculated for both temperature conditions:

For 25°C:

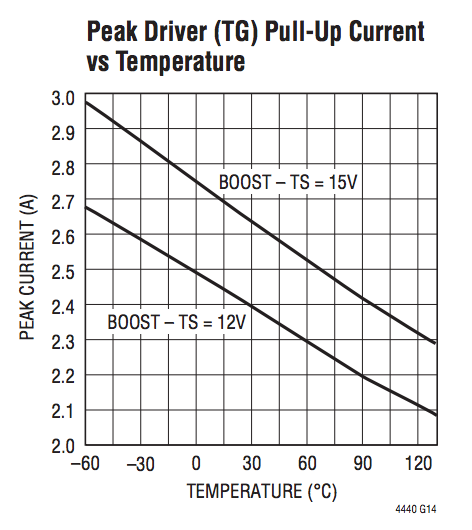
And for 125°C:



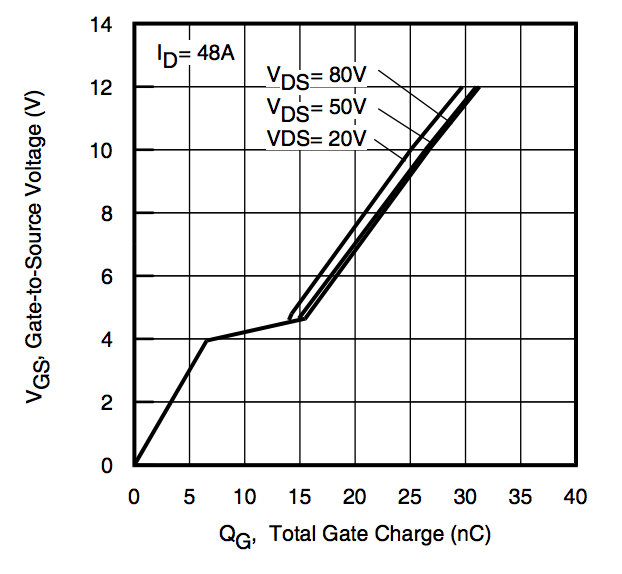
**Figure 5 –** IRFH7191 RDS(on) vs. VGS at 25°C and 125°C.

Analysis of switching losses in the linear region is more complicated, as there are many sources of switching losses [4]. The following sources of switching losses may be calculated with the parameters of the MOSFET which are made available from the manufacturer: turn-off losses, turn-on losses, body diode recovery losses, gate charge losses, and output capacitance losses. These losses are also closely related to the characteristics of the driver circuit; a more powerful driver circuit will reduce the time the MOSFET operates in the linear region.

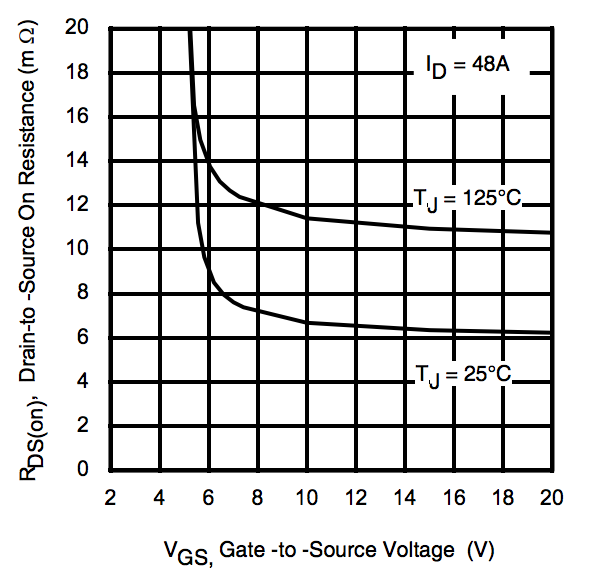
For the purposes of these analyses, a 2.4A peak driver pull-up current will be assumed, based on typical performances of the LTC4440 high-side high-speed driver IC (see figure 6) [10]. Furthermore, the MOSFET transitions through the linear region as the gate driver removes charge from the MOSFET’s gate. The charge at the gate is related to the MOSFET’s gate to source voltage by the curve shown in figure 7. Note that this is not a purely linear relationship, therefore for turn-on and turn-off losses in the MOSFET, it is useful to analize the MOSFET’s transition in three stages (corresponding to the three linear pieces of the curve in figure 7). Furthermore, the on-state resistance of the MOSFET’s channel is related to the gate-to-source voltage by the curve in figure 8.



**Figure 6 –** Peak Driver Pull-Up Current for the LTC-4440 High-Side MOSFET Driver.



**Figure 7 –** MOSFET Gate-to-Source Voltage vs. Gate Charge; Plateau due to the Miller Effect.



**Figure 8 –** MOSFET On-State Resistance vs. Gate-To-Source Voltage.

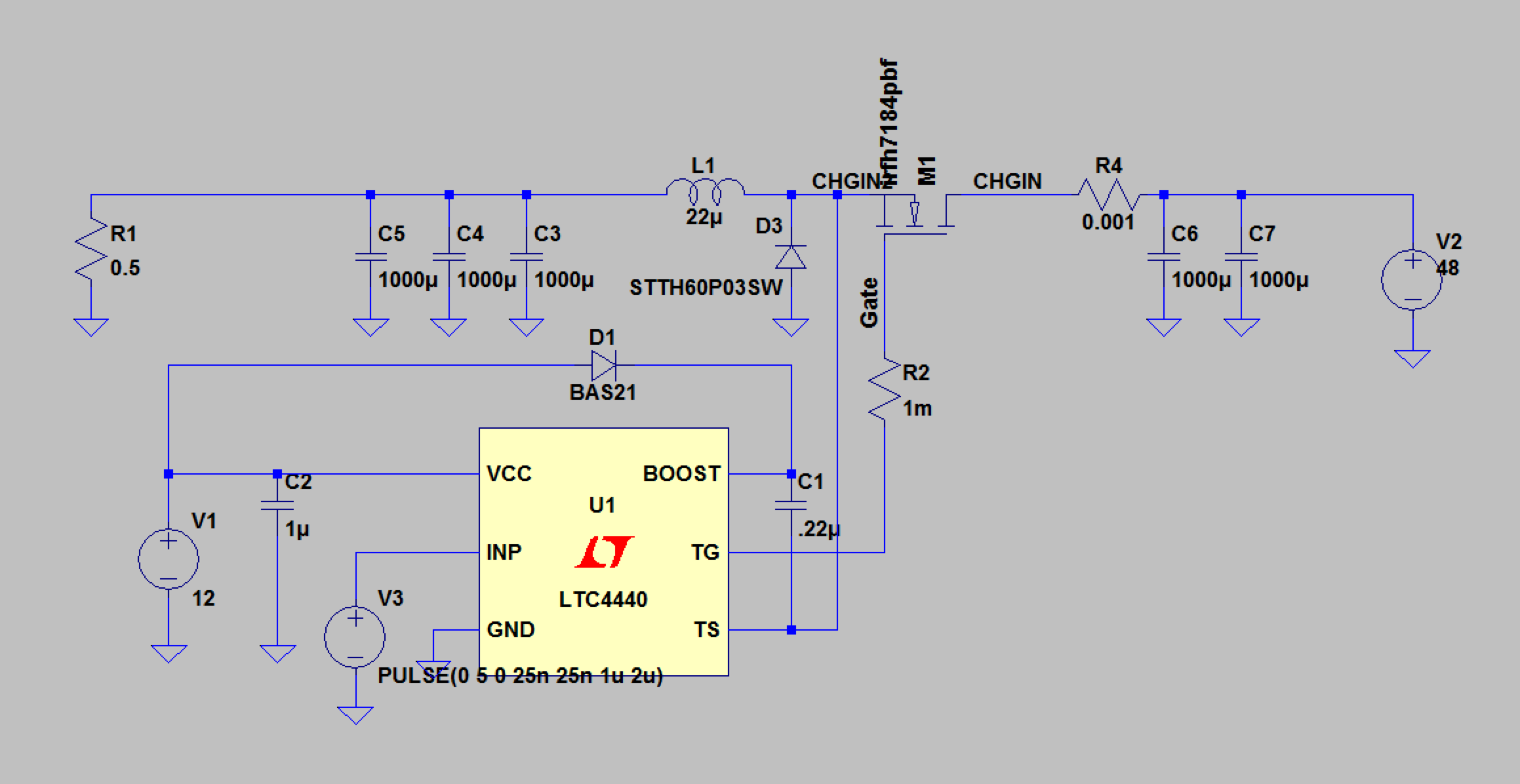
Thus with the curves in figures 7 and 8 it is possible to determine the MOSFET’s turn-on and turn-off losses [4]. First is the analysis of the three stages of the MOSFET’s turn-off period.

The first stage consists of the MOSFET’s transition from its high on-state gate-to-source voltage (sustained by the gate driver circuit and the MOSFET’s gate capacitance) to the knee in the curves of figures 7 and 8, which is VGS ≈ 6V. Figure shows that during this transition period RDS(on) remains approximately the same as in the MOSFET’s saturation operation region, therefore the losses here are the same as for the MOSFET’s on-state. This period of the switching is still key; however, as a significant portion of the gate charge is dissipated in this period, leading to the second stage of the turn-off period.

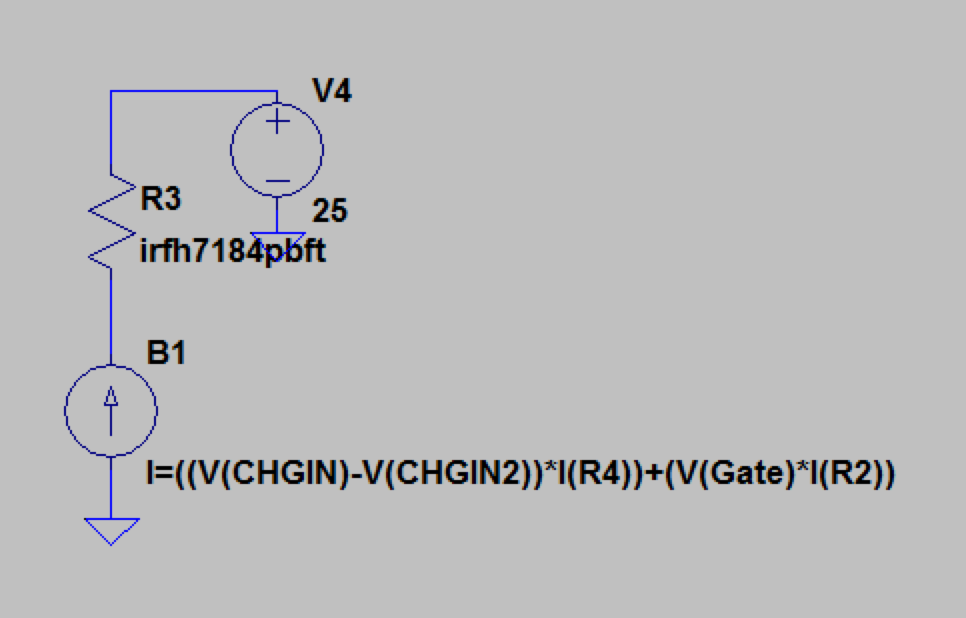
In the second stage of the MOSFET’s

**SPICE Model Simulations**

As there is a complex interdependence between switching losses, MOSFET heating, MOSFET gate charge, and MOSFET driver current, a SPICE model of the charger circuitry was created to simulate its electrical and thermal characteristics. The model simulations were run using the LTSpice software [9]. The simulation consisted of a buck-converter with models of real-world components, including the LTC4440 MOSFET driver IC. Additionally, MOSFET thermal-analysis was conducted under various circuit loading conditions using MOSFET thermal models provided by the manufacturers. The basic circuit network used for the electrical simulation is show in figure 5, while a basic thermal model is shown in figure 6. It is important to note that the components (such as the MOSFET thermal impedance) in some of these networks are actually macromodels of more complex networks not presented immediately in those figures.



**Figure 5 –** Buck Converter SPICE network in LTSpice.



**Figure 6 –** MOSFET Thermal model SPICE network in LTSpice.

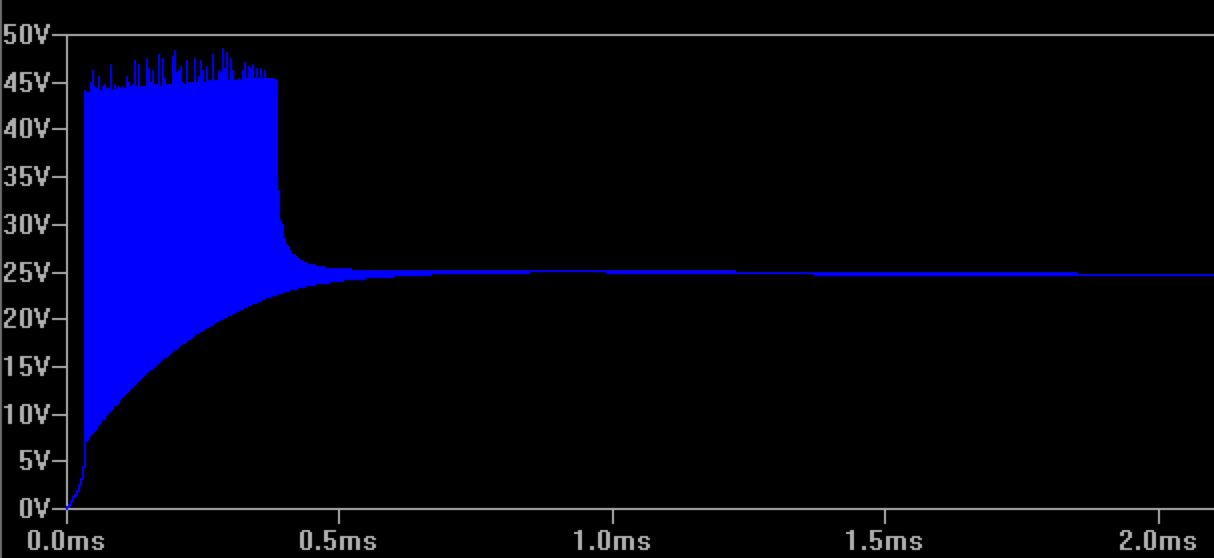
The initial model developed was a simple model for conducting baseline tests of various MOSFETs and for verifying model accuracy compared to expected results. Components of the electrical model include the non-ideal inductor L1, ideal filter capacitors with a non-zero ESR, ideal voltage sources for circuit power supply, non-ideal diode models, complex MOSFET models, and a macromodel of the driver IC provided by the manufacturer [10].

The thermal model varied depending on the data provided by the manufacturer. For the International Rectifier MOSFETs, a Foster RC thermal model was used for transient analysis, as the necessary parameters for this model were provided by the manufacturer [6][7][8]. This macromodel was represented by the two-terminal network element R3 (see figure 6). An arbitrary current source (B1) based on the power loss in the MOSFET was used to simulate a heat source, and a DC voltage source (V4) was used to model ambient temperature [11].

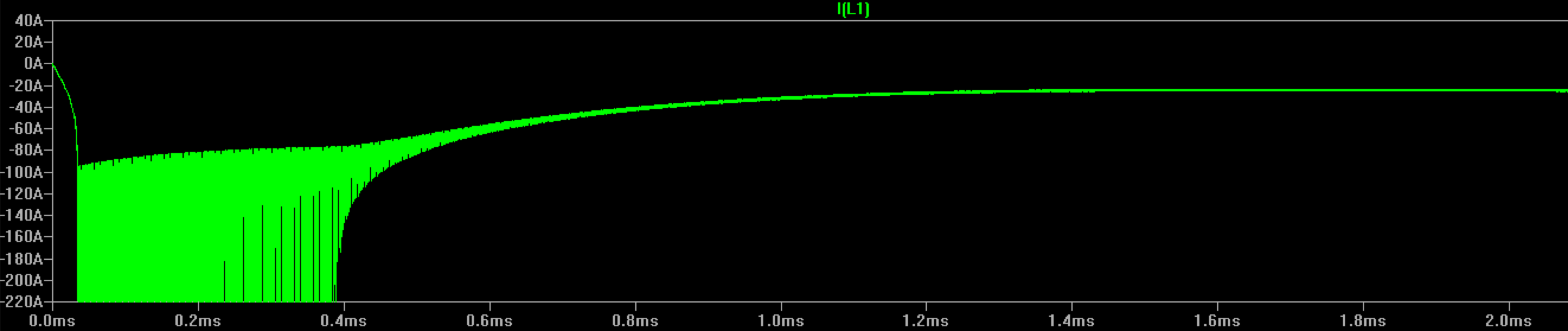
A vary of design parameters were tested using SPICE simulations, including inductance values, various MOSFETs, filter capacitance, and inductor saturation characteristics. The follow spice tests were conducted to characterize the circuit:

*Test 1: Basic Model Performance*

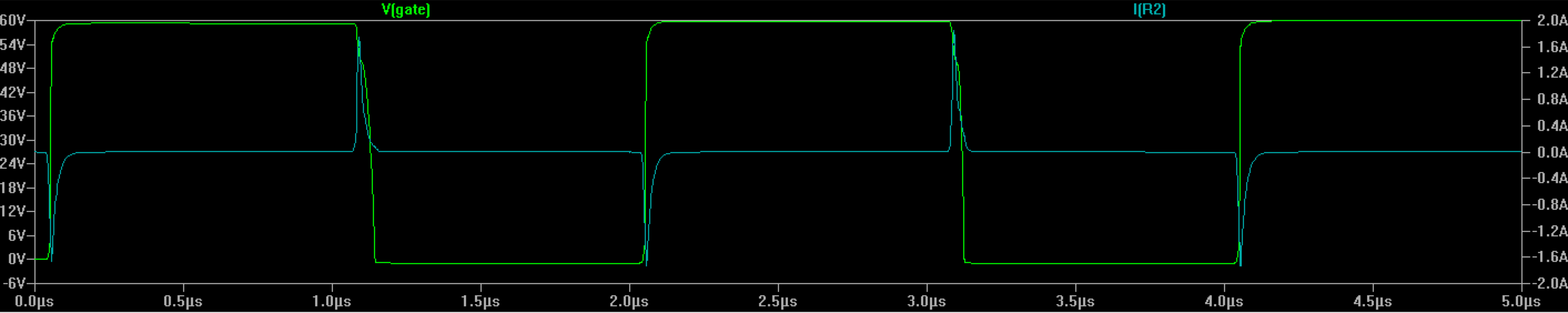
The first tests conducted were simple operation of the converter with a resistive load to verify that the simulation’s nets and models were configured properly. A 48V source was used as the input voltage, with a 500kHz driver signal at 50% duty cycle, in order to provide an expected 24V output to a 1.0-Ohm load. The results of the simulation are presented in figure 7 below.



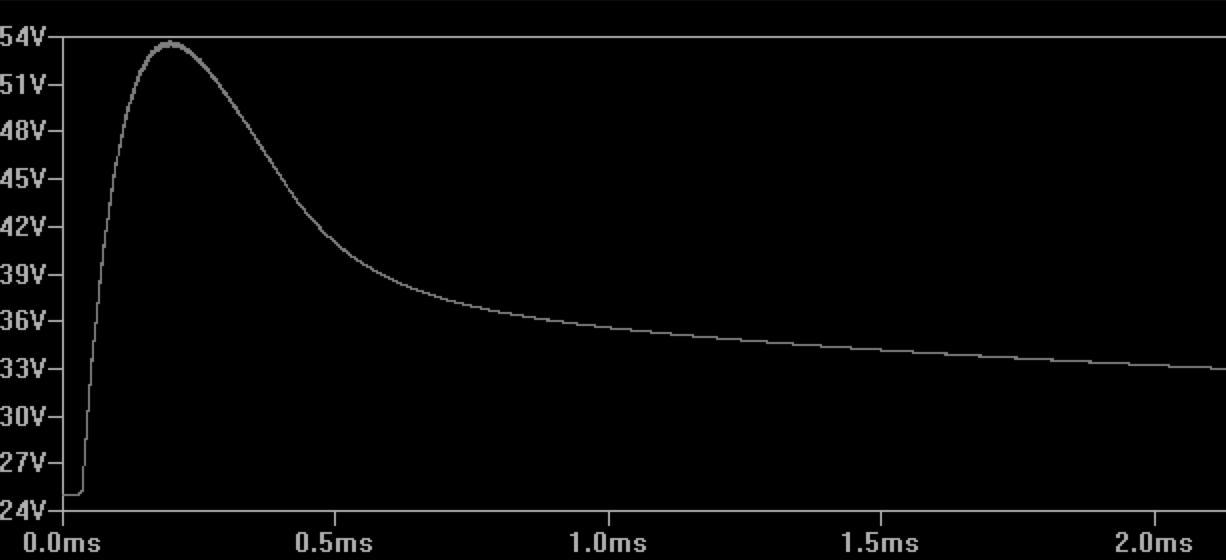
**Figure 7 –** Buck-Converter Output Voltage on Startup (Transient Analysis).



**Figure 8 –** Buck-Converter Inductor Current on Startup (Transient Analysis).



**Figure 9 –** Buck-Converter MOSFET Driver Current (Cyan Trace) and MOSFET Gate Voltage (Green Trace).



**Figure 10 –** MOSFET Junction Temperature in Degrees Celsius.



**Figure 11 –** Output Voltage for Various Driver Duty Cycles.

*Test 2: MOSFET Thermal Analysis in Various Load Conditions*

A basic thermal model for the

*Test 3: Basic MOSFET Performance Characterizations*

*Test 4: Load Transient Simulations*

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